UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,853	02/19/2004	Shrjie Tzeng	58268.00305	2472

32294 7590 06/27/2008

SQUIRE, SANDERS & DEMPSEY L.L.P.
8000 TOWERS CRESCENT DRIVE
14TH FLOOR
VIENNA, VA 22182-6212

EXAMINER	
TURNER, ASHLEY D	

ART UNIT	PAPER NUMBER
2154	

MAIL DATE	DELIVERY MODE
06/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,853	TZENG ET AL.	
	Examiner	Art Unit	
	ASHLEY D. TURNER	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19 are rejected under 35 U.S.C. 103 (a) as being unpatentable over et al Kadambi (US 6,560,229) in view of Goyal (US 6,466,985 B1).

Regarding claim 1

Referring to claim 1 Kadambi discloses a method of handling datagrams in a network device coupled to other network devices, said method comprising: receiving an incoming datagram at a port of the network device (Col. 3 lines 15-24 The method comprises the steps of receiving an incoming packet at a first port) ; determining an egress port for the incoming datagram based on a destination address contained in the incoming datagram and a lookup of an address resolution lookup (ARL) table ; performing a lookup of ARL table based on a source address contained in the incoming datagram to determine whether the source address has been learned previously (Col.3 lines 15-30 The invention also includes a method of switching data in a network switch.

The method comprises the steps of receiving an incoming packet at a first port, then reading a first packet portion, less than a full packet length, to determine particular packet information. The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table. If a match is made, the packet is modified to include appropriate forwarding and routing information based on the matching entry). ; determining whether the other network devices have learned the source address when the source has been learned previously (Col.3 lines 15-30 The invention also includes a method of switching data in a network switch. The method comprises the steps of receiving an incoming packet at a first port, then reading a first packet portion, less than a full packet length, to determine particular packet information. The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table. If a match is made, the packet is modified to include appropriate forwarding and routing information based on the matching entry). Kambi did not disclose continuing to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address. The general concept of continuing to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address is well known in the art as taught by Goyal. Goyal discloses continuing to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address.

(Col. 4 lines 46 -67 There are four aspects of constructing a flow: (1) declaring a name; (2) pinning the route, (3) enabling reverse path routing, and (4) assigning attributes (such as QoS). Abstractly, current network nodes maintain two tables, a routing table and a forwarding table. In the case of a traditional router the forwarding table corresponds to the routing cache. On an ATM switch or an MPLS Label Switch Router (LSR), the forwarding table is respectively the Virtual Channel (VC) lookup table or the label lookup table. To support the flows used in the embodiments of the invention, a traditional router would be augmented with an additional forwarding table for mapping flow names to flow state (including the output port), as discussed in more detail with reference to FIG. 2. A flow request may be interpreted as an implicit request for route pinning. If not, route pinning may be requested subsequently in a separate message. Without route pinning, the entry in the flow cache simply points to the corresponding entry (in the regular cache) for the destination address. When route pinning is requested this entry is copied and thus becomes independent of changes in the default destination based route.) It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kadambi to include continuing to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address in order to provide physical connection to one or more network links.

Regarding claim 8

Claim 8 is similarly rejected using at least the same reasoning/ citations provided above for claim 1 since they recite the same limitations and are distinguished only by statutory category.

Regarding claim 2

Referring to claim 2 Kadambi and Goyal discloses all the limitations of claim 2 which is described above. Kadambi also discloses wherein the method further comprises updating a hit bit in the ARL table when the source address has been learned previously (Col. 3 lines 1-10 One of the first data port interface and the second data port interface is configured to update the address resolution lookup table based upon newly learned layer two addresses. An update to an address table associated with an initial data port interface of the first and second data port interfaces results in the initial data port interface sending a synchronization signal to other address resolution tables in the network switch. Therefore, all address resolution tables on the network switch are synchronized on a per entry basis. A learning and an accessing of an address in the address resolution lookup table results in the setting of a hit bit).

Regarding claim 9

Claim 9 is similarly rejected using at least the same reasoning/ citations provided above for claim 2 since they recite the same limitations and are distinguished only by statutory category.

Regarding claim 3

Referring to claim 3 Kadambi and Goyal discloses all the limitations of claim 3 which is described above. Kadambi also discloses wherein the step of determining whether the other network devices have learned the source address comprises examining a learned all devices tag for the source address in the ARL table (Col 18 lines 20- 28 The ARL engine 143 reads the packet; if the packet has a VLAN tag according to IEEE Standard 802.1q, then ARL engine 143 performs a look-up based upon tagged VLAN table 231, which is part of VLAN table 23. If the packet does not contain this tag, then the ARL engine performs VLAN lookup based upon the port based VLAN table 232. Once the VLAN is identified for the incoming packet, ARL engine 143 performs an ARL table searched based upon the source MAC address and the destination MAC address).

Regarding claim 10

Claim 10 is similarly rejected using at least the same reasoning/ citations provided above for claim 3 since they recite the same limitations and are distinguished only by statutory category.

Regarding claim 4

Referring to claim 4 Kadambi and Goyal discloses all the limitations of claim 4 which is described above. Kadambi also discloses wherein the network device and the other devices are connected through a ringed connection and the step of continuing to relay a learning message comprises continuing to relay a learning message through the ringed connection. (Col. 1 lines 15-23 The invention relates to a method and apparatus for high performance switching in local area communications networks such as token ring, ATM, ethernet, fast ethernet, and gigabit ethernet environments, generally known as LANs. In particular, the invention relates to a new switching architecture in an integrated, modular, single chip solution, which can be implemented on a semiconductor substrate such as a silicon chip). and (Col. 3 lines 5-17 One of the first data port interface and the second data port interface is configured to update the address resolution lookup table based upon newly learned layer two addresses. An update to an address table associated with an initial data port interface of the first and second data port interfaces results in the initial data port interface sending a synchronization signal to other address resolution tables in the network switch. Therefore, all address resolution tables on the network switch are synchronized on a per entry basis. A learning and an accessing of an address in the address resolution lookup table results in the setting of a hit bit).

Regarding claim 11

Claim 11 is similarly rejected using at least the same reasoning/ citations provided above for claim 4 since they recite the same limitations and are distinguished only by statutory category.

Regarding claim 5

Referring to claim 5 Kadambi and Goyal discloses all the limitations of claim 5 which is described above. Kadambi also discloses wherein the method steps are also performed in the other network devices (Col. 4 lines 31-61 FIG. 1 illustrates a configuration wherein a switch-on-chip (SOC) 10, in accordance with the present invention, is functionally connected to external devices 11, external memory 12, fast ethernet ports 13, and gigabit ethernet ports 15. For the purposes of this embodiment, fast ethernet ports 13 will be considered low speed ethernet ports, since they are capable of operating at speeds ranging from 10 Mbps to 100 Mbps, while the gigabit ethernet ports 15, which are high speed ethernet ports, are capable of operating at 1000 Mbps. External devices 11 could include other switching devices for expanding switching capabilities, or other devices as may be required by a particular application. External memory 12 is additional off-chip memory, which is in addition to internal memory which is located on SOC 10, as will be discussed below. CPU 52 can be used as necessary to program SOC 10 with rules which are appropriate to control packet processing. However, once SOC 10 is appropriately programmed or configured, SOC 10 operates,

as much as possible, in a free running manner without communicating with CPU 52. Because CPU 52 does not control every aspect of the operation of SOC 10, CPU 52 performance requirements, at least with respect to SOC 10, are fairly low. A less powerful and therefore less expensive CPU 52 can therefore be used when compared to known network switches. As also will be discussed below, SOC 10 utilizes external memory 12 in an efficient manner so that the cost and performance requirements of memory 12 can be reduced. Internal memory on SOC 10, as will be discussed below, is also configured to maximize switching throughput and minimize costs).

Regarding claim 6

Referring to claim 6 Kadambi and Goyal discloses all the limitations of claim 6 which is described above. Kadambi also discloses wherein the step of determining an egress port comprises flooding all ports of the network device with the incoming datagram when the lookup of the ARL table does not find a match with the destination address (Col.3 lines 21-30 The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table. If a match is made, the packet is modified to include appropriate forwarding and routing information based on the matching entry. The packet is then sent on a communication channel to a selected memory buffer. If there is no match, the particular packet information is learned and placed as a second entry in the

lookup table. The packet information is modified to indicate that the packet is to be sent to all ports on the network switch).

Regarding claim 13

Claim 13 is similarly rejected using at least the same reasoning/ citations provided above for claim 6 since they recite the same limitations and are distinguished only by statutory category.

Regarding claim 7

Referring to claim 7 Kadambi and Goyal discloses all the limitations of claim 7 which is described above. Kadambi also discloses wherein the step of receiving an incoming datagram comprises receiving an incoming data packet (Col. 3 lines 16-22The method comprises the steps of receiving an incoming packet at a first port, then reading a first packet portion, less than a full packet length, to determine particular packet information. The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table).

Regarding claim 12

Referring to claim 12 Kadambi and Goyal discloses all the limitations of claim 12 which is described above. Kadambi also discloses wherein the network device is connected to the other network device through one of a stacking port i.e. port 13 and an expansion port i.e. port 15 of the network device (Col. 4 lines 31-61 FIG. 1 illustrates a configuration wherein a switch-on-chip (SOC) 10, in accordance with the present invention, is functionally connected to external devices 11, external memory 12, fast ethernet ports 13, and gigabit ethernet ports 15. For the purposes of this embodiment, fast ethernet ports 13 will be considered low speed ethernet ports, since they are capable of operating at speeds ranging from 10 Mbps to 100 Mbps, while the gigabit ethernet ports 15, which are high speed ethernet ports, are capable of operating at 1000 Mbps. External devices 11 could include other switching devices for expanding switching capabilities, or other devices as may be required by a particular application. External memory 12 is additional off-chip memory, which is in addition to internal memory which is located on SOC 10, as will be discussed below. CPU 52 can be used as necessary to program SOC 10 with rules which are appropriate to control packet processing. However, once SOC 10 is appropriately programmed or configured, SOC 10 operates, as much as possible, in a free running manner without communicating with CPU 52. Because CPU 52 does not control every aspect of the operation of SOC 10, CPU 52 performance requirements, at least with respect to SOC 10, are fairly low. A less powerful and therefore less expensive CPU 52 can therefore be used when compared to known network switches. As also will be discussed below, SOC 10 utilizes external memory 12 in an efficient manner so that the cost and performance

requirements of memory 12 can be reduced. Internal memory on SOC 10, as will be discussed below, is also configured to maximize switching throughput and minimize costs).

Regarding claim 14

Referring to claim 14 Kadambi and Goyal discloses a network device coupled to other network devices for handling datagrams comprising: a plurality of ports receiving an incoming datagram (Col. 3 lines 16-24 The method comprises the steps of receiving an incoming packet at a first port) ; an address resolution lookup (ARL) table; an egress port determiner for determining an egress port for the incoming datagram based on a destination address contained in the incoming datagram; an ARL table reader for performing a lookup of ARL table based on a source address contained in the incoming datagram to determine whether the source address has been learned previously (Col.3 lines 16-24 The invention also includes a method of switching data in a network switch. The method comprises the steps of receiving an incoming packet at a first port, then reading a first packet portion, less than a full packet length, to determine particular packet information. The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table. If a match is made, the packet is modified to include appropriate forwarding and routing information based on the matching entry). ; An ARL table writer for writing an entry into the ARL table when the source address has not

been learned previously, a global address determiner for determining whether the other network devices have learned the source address when the source has been learned previously (Col.3 lines 16-24 The invention also includes a method of switching data in a network switch. The method comprises the steps of receiving an incoming packet at a first port, then reading a first packet portion, less than a full packet length, to determine particular packet information. The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table. If a match is made, the packet is modified to include appropriate forwarding and routing information based on the matching entry). Kambi did not disclose a learning message forwarder to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address. The general concept of a learning message forwarder to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address is well known in the art as taught by Goyal. Goyal discloses a learning message forwarder to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address. (Col. 4 lines 46 -67 There are four aspects of constructing a flow: (1) declaring a name; (2) pinning the route, (3) enabling reverse path routing, and (4) assigning attributes (such as QoS). Abstractly, current network nodes maintain two tables, a routing table and a forwarding table. In the case of a traditional router the forwarding table corresponds to the routing cache. On an ATM switch or an MPLS Label

Switch Router (LSR), the forwarding table is respectively the Virtual Channel (VC) lookup table or the label lookup table. To support the flows used in the embodiments of the invention, a traditional router would be augmented with an additional forwarding table for mapping flow names to flow state (including the output port), as discussed in more detail with reference to FIG. 2. A flow request may be interpreted as an implicit request for route pinning. If not, route pinning may be requested subsequently in a separate message. Without route pinning, the entry in the flow cache simply points to the corresponding entry (in the regular cache) for the destination address. When route pinning is requested this entry is copied and thus becomes independent of changes in the default destination based route.) It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kadambi to include a learning message forwarder to relay a learning message with the source address to the other network devices when it is determined that the other network devices have not learned the source address in order to provide physical connection to one or more network links.

Regarding claim 15

Referring to claim 15 Kadambi and Goyal discloses all the limitations of claim 15 which is described above. Kadambi also discloses an updater for updating a hit bit in the ARL table when the source address has been learned previously (Col. 3 lines 1-10 One of the first data port interface and the second data port interface is configured to update

the address resolution lookup table based upon newly learned layer two addresses. An update to an address table associated with an initial data port interface of the first and second data port interfaces results in the initial data port interface sending a synchronization signal to other address resolution tables in the network switch. Therefore, all address resolution tables on the network switch are synchronized on a per entry basis. A learning and an accessing of an address in the address resolution lookup table results in the setting of a hit bit).

Regarding claim 18

Claim 18 is similarly rejected using at least the same reasoning/ citations provided above for claim 6 since they recite the same limitations and are distinguished only by statutory category.

Regarding claim 16

Referring to claim 16 Kadambi and Goyal discloses all the limitations of claim 16 which is described above. Kadambi also discloses wherein the global address determiner comprises an examiner for examining a learned all devices tag for the source address in the ARL table (Col 18 lines 20- 28 The ARL engine 143 reads the packet; if the packet has a VLAN tag according to IEEE Standard 802.1q, then ARL engine 143 performs a

look-up based upon tagged VLAN table 231, which is part of VLAN table 23. If the packet does not contain this tag, then the ARL engine performs VLAN lookup based upon the port based VLAN table 232. Once the VLAN is identified for the incoming packet, ARL engine 143 performs an ARL table searched based upon the source MAC address and the destination MAC address).

Regarding claim 19

Referring to claim 19 Kadambi and Goyal discloses all the limitations of claim 19 which is described above. Kadambi also discloses wherein an egress port determiner comprises a port flooder for flooding all ports of the network device with the incoming datagram when the lookup of the ARL table does not find a match with the destination address (Col.3 lines 21-30 The particular packet information includes a source address and a destination address. The particular packet information is compared to information contained in a lookup table. If a match is made, the packet is modified to include appropriate forwarding and routing information based on the matching entry. The packet is then sent on a communication channel to a selected memory buffer. If there is no match, the particular packet information is learned and placed as a second entry in the lookup table. The packet information is modified to indicate that the packet is to be sent to all ports on the network switch).

Response to Arguments

Applicant's arguments filed on 4/17/2008 have been fully considered but they are deemed moot in view of the new grounds of rejections.

Conclusion

Arguments are deemed moot in view of the new grounds of rejection necessitated by the amendment.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashley D. Turner whose telephone number is 571-270-1603. The examiner can normally be reached on Monday thru Friday 7:30a.m.-5:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ashley D Turner
Examiner
Art Unit 2154

/Nathan J. Flynn/

Supervisory Patent Examiner, Art Unit 2154